REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 24 August 2005. Responsive to the Examiner's rejections, Claims 1, 7, 9, and 12 have been amended and are now believed to be clearer in their respective recitations. Claims 4-6, 8, 10, 11 and 15 have been cancelled by this Amendment and Claims 16-20 have been appended for prosecution. Upon entry of this Amendment, Claims 1-3, 7, 9, 12-14 and 16-20 will be pending in the Application.

In the Official Action, the Examiner rejected Claim 1 and, by dependency, Claims 2-6, under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as Applicant's invention. The Examiner gave as grounds for the rejection that "Claim 1, failed to point out the function of the interconnected elements as being indefinite". Although it is unclear as to what is meant by the Examiner's stated grounds for rejection, Claim 1 has been amended and is believed to now unambiguously recite the combination of elements considered by the Applicant to be the invention of the subject Patent Application.

The Examiner rejected Claims 1-3, 6-7 and 12-15 under 25 U.S.C. § 102(e) as being anticipated by Sakaguchi (U.S. Patent # 6,490,057). In setting forth this rejection, the Examiner cited Sakaguchi's horizontal scanning thinned-out pulse

generator as fulfilling the claimed shifting device and cited Sakaguchi's clock changeover section as fulfilling the claimed addition device. The Examiner further correlated Sakaguchi's A/D converter and the claimed input conducting wire and stated that one end of the addition device, as met by Sakaguchi's clock changeover section, is coupled to the claimed input conducting wire, as met by Sakaguchi's A/D converter.

The Examiner merely objected to Claims 4-5 and 8-11 as being dependent upon a rejected base claim and stated that the Claims would be allowable if rewritten in independent form to include the limitations of the base Claim and any intervening Claims. The Examiner stated that the prior art of record does not show certain claimed features of the invention that are limited by a function of $\log_2 n$, where n is at least 2^i more than the number of bits of signal and i is an integer.

Applicant's invention is directed to applying a scaling factor to a horizontal scan of a scanner. As amended Claim 7 now more clearly recites, a method consistent with the invention provides "an input signal including a sequence of pixel values, each of said pixel values being represented by a predetermined number of bits". The method proceeds by "right-shifting said input signal t bits to produce a shifted signal" and then "adding said input signal and said shifted signal to produce a summed signal". The method continues by "incrementing the value of t" and then "right-shifting said summed signal a number of bits equal to the

value of *t* to produce a t-shifted signal". After "adding said summed signal to said t-shifted signal to produce a new summed signal", the process is iterated by "repeating the method at said value of *t* incrementing step with said new summed signal as said summed signal". The iterations continue "until a predetermined number of cycles have been executed". The process is concluded by "right-shifting said summed signal 2 bits to produce an output signal".

Applicant's invention may be alternatively defined in terms of configurations of system components. In a first configuration, as recited by Claim 1, as now amended, and exemplified in the diagram of Fig. 1, "a switching device having a first input terminal and a second input terminal" is provided, which "receiv[es] at said first input terminal thereof an input signal including a number of bits". The switching device selects "a signal selected from said input signal and a second signal responsive to a first clock cycle number". The system includes "an addition device having a first input terminal and a second input terminal and operable to produce at an output terminal thereof a sum of a signal provided to said first input terminal and a signal provided to said second input terminal". The output terminal of the addition device is "coupled to said second input terminal of said switching device and providing thereto said second signal". Also included in the system is "a shifting device having an input terminal coupled to said output terminal of said switching device and having an output terminal coupled to said second input terminal of said addition device". The output of the shifting device is

"said selected signal shifted a number of bits corresponding to a clock cycle number", which is provided to "an output terminal" to provide "an output signal upon a second clock cycle number".

An exemplary embodiment of a second configuration is illustrated in Fig. 3. As amended Claim 12 now more clearly recites, the system includes "at least an adder connected to [an] input" and "at least a shifter with an input terminal thereof connected to said input and an output terminal thereof connected to an input of said adder". Also included is "an end shifter with an input terminal thereof connected to said adder and an output terminal thereof connected to an output operable to produce thereat an output signal".

These and other features now more clearly recited by Applicant's pending claims are nowhere found in the cited prior art. Sakaguchi's teachings are directed to the "pixel-abstraction method" described as inferior prior art in the subject Patent Application. As such, components even partially adequate for carrying out Applicant's invention are not disclosed, or even suggested by the reference. Indeed, the clock changeover unit of Sakaguchi, cited by the Examiner as being an addition device does not add signals together, but rather selects one of two clock signals for timing the image capture in accordance with a horizontal scale factor. Further, the horizontal scanning thinned-out pulse generator cited by the Examiner as fulfilling the function of a shifter does not perform bit-shifting operations, but is rather a waveform generator for purposes of controlling which pixels in the

horizontal scan line are retained in a scaled image.

Nowhere in the cited reference is it shown, or even suggested, the step of "right-shifting said input signal *t* bits to produce a shifted signal". Nor does the reference disclose or suggest "adding said input signal and said shifted signal to produce a summed signal". Thus, as the reference fails to show each and every element or method step of Applicant's invention, as now claimed, it is respectfully submitted that Sakaguchi cannot anticipate the invention of the subject Patent Application. Further, as the reference does not show or suggest the unique combination of method steps and associated components for the purposes and objectives set forth in the subject Patent Application, the reference cannot make obvious the invention, as now claimed.

The independent Claims of the subject Patent Application, as now amended, recite steps and elements not disclosed or suggested by the prior art of record and are thus believed to be allowable. The dependent Claims recite the limitations of the Claims from which they depend and are therefore believed to be allowable for at least the same reasons for which their corresponding base claims are allowable.

The remaining references cited by the Examiner but not used in the rejections have been reviewed, but are believed to be further remote from the subject matter of the subject Patent Application then the Patent cited when patentable considerations are taken into account.

The subject Patent Application is now believed to be allowable and such action is respectfully requested.

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